WHAT IS CLAIMED IS:

1. FIR filter apparatus comprising:

an input for receiving an input signal;

an FIR filter comprising a plurality of filter stages; and

a delay coupled between two of said plurality of filter stages to delay application of the input signal to at least one of said filter stages to skip filtering a portion of the input signal.

2. Apparatus according to Claim 1, wherein the delay of said delay is adjustable.

3. Apparatus according to Claim 1, wherein the plurality of filter stages comprises a first plurality of stages and a second plurality of stages, the first plurality of stages receiving a predetermined first portion of the input signal, said delay providing a variable second portion of the input signal to said second plurality of stages.

4. Apparatus according to Claim 3, further comprising a memory storing a delay value for application to said delay.

5. Apparatus according to Claim 3, wherein said first plurality of filter stages comprises a plurality of filter blocks, each having a plurality of taps, and wherein said second plurality of stages comprises at least one filter block having a plurality of taps, and further comprising:

a first plurality of LMS engines which provide a first plurality of weighting coefficients to the taps of said plurality of filter blocks; and

a second LMS engine which provides a second plurality of weighting coefficients to the taps of said at least one filter block.

6. Apparatus according to Claim 5, wherein said plurality of filter blocks comprises four filter blocks each having 32 taps, and wherein said at least one filter block comprises one filter block having 32 taps.

7. FIR filter apparatus comprising:

a signal input receiving an input signal;

a first block of filter stages having a respective first plurality of taps which receive a respective first plurality of weighting coefficients, for filtering a first portion of the input signal in accordance with the first plurality of weighting coefficients;

a second block of filter stages having a respective second plurality of taps which receive a respective second plurality of weighting coefficients, for filtering a second portion of the input signal in accordance with the second plurality of weighting coefficients; and

a delay which variably delays application of the second portion of the input signal to the second block of filter stages with respect to the first portion of the input signal.

8. An FIR filter comprising:

a plurality of delay elements; and

a plurality of coefficient taps, each associated with a portion of an input signal in corresponding stages of delay from a corresponding delay element,

wherein at least one delay element has a period of delay that is selectable.

9. An FIR filter according to Claim 8, wherein the selectable period of delay is selectable independently of a period of delay for other delay elements.

10. An FIR filter according to Claim 9, wherein each delay element has a minimum period of delay, and wherein the selectable period of delay is adjustable to be greater than the minimum period of delay.

11. An FIR filter according to Claim 8, wherein the FIR filter further includes pin-out arrangements for setting the selectable period of delay.

12. FIR filter apparatus comprising:

input means for receiving an input signal;

filter means for filtering the input signal and having a plurality of filter stages; and

delay means coupled between two of said plurality of filter stages for delaying application of the input signal to at least one of said filter stages to skip filtering a portion of the input signal.

13. FIR filter apparatus comprising:

signal input means for receiving an input signal;

a first block of filter means, having a respective first plurality of taps which receive a respective first plurality of weighting coefficients, for filtering a first portion of the input signal in accordance with the first plurality of weighting coefficients;

a second block of filter means, having a respective second plurality of taps which receive a respective second plurality of weighting coefficients, for

filtering a second portion of the input signal in accordance with the second plurality of weighting coefficients; and

delay means for adjustably delaying application of the second portion of the input signal to the second block of filter means with respect to the first portion of the input signal.

14. An echo canceller comprising:

an input for receiving an input signal having an echo;

an FIR filter including:

(i) a first plurality of filter stages comprising a plurality of filter blocks, each having a plurality of taps; and

(ii) a second plurality of stages comprising at least one filter block having a plurality of taps;

a first plurality of LMS engines which provide a first plurality of weighting coefficients to the taps of said plurality of filter blocks;

a second LMS engine which provides a second plurality of weighting coefficients to the taps of said at least one filter block to filter said echo; and

a delay coupled between said plurality of filter blocks and said at least on filter block to delay application of the input signal to said at least one filter block to skip filtering a portion of the input signal which contains negligible echo.

15. An Ethernet transceiver, comprising:

an input for inputting an input signal into an Ethernet cable;

an output for outputting an output signal from the Ethernet cable, the output signal corresponding to the input signal and having an echo;

an FIR filter including:

(i) a first plurality of filter stages comprising a plurality of filter blocks, each having a plurality of taps; and

(ii) a second plurality of stages comprising at least one filter block having a plurality of taps;

a first plurality of LMS engines which provide a first plurality of weighting coefficients to the taps of said plurality of filter blocks;

a second LMS engine which provides a second plurality of weighting coefficients to the taps of said at least one filter block to filter said echo; and

a delay coupled between said plurality of filter blocks and said at least on filter block to delay application of the output signal to said at least one filter block to skip filtering a portion of the output signal which contains negligible echo.

16. A transceiver according to Claim 15, wherein said first plurality of LMS engines includes:

a first set of LMS engines applying weighting coefficients to a first filter block; and

a second set of LMS engines respectively applying weighting coefficients to a corresponding number of filter blocks.

17. A method for controlling an FIR filter comprising the steps of:

receiving an input signal;

filtering the input signal with an FIR filter having a plurality of filter stages; and

delaying application of the input signal to at least one of said filter stages with respect to the other filter stages to skip filtering a portion of the input signal.

18. A method of controlling an FIR filter comprising the steps of:

receiving an input signal;

filtering a first portion of the input signal with a first block of filter stages having a respective first plurality of taps which receive a respective first plurality of weighting coefficients, the first portion of the input signal being filtered in accordance with the first plurality of weighting coefficients;

filtering a second portion of the input signal with a second block of filter stages having a respective second plurality of taps which receive a respective second plurality of weighting coefficients, the second portion of the input signal being filtered in accordance with the second plurality of weighting coefficients; and

adjustably delaying application of the second portion of the input signal to the second block of filter stages with respect to the first portion of the input signal.

19. A method for selecting a period of delay in an FIR filter having (i) a plurality of delay elements and (ii) a plurality of coefficient taps each associated with a portion of an input signal in corresponding stages of delay from a corresponding delay element, in which at least one delay element has a period of delay that is selectable, the method comprising the steps of:

measuring components of an input signal so as to identify a sequence of components that are smaller than another sequence of larger components; and

setting the selectable period of delay to prevent application of the identified sequence of smaller components of the input signal to the coefficient taps.

20. A method according to Claim 19, further comprising the step of transmitting a test signal, wherein the input signal comprises an echo of the test signal.

21. A method according to Claim 19, wherein said steps of measuring and setting are applied iteratively with a different setting for the selectable period of delay so as to identify the sequence of smaller components.

22. FIR filter apparatus comprising:

an input responsive to an input signal;

an FIR filter comprising three filter stages; and

a first delay circuit having a first time delay coupled between two of said three filter stages;

a second delay circuit having a second time delay coupled between another two of said three filter stages, wherein the first time delay and second time delay are different.

23. An apparatus according to Claim 22, wherein the second time delay of said second delay circuit is adjustable.

24. An apparatus according to Claim 22, further comprising a selector in communication with said second delay circuit to adjust the second time delay.

25. FIR filter apparatus comprising:

a first plurality of stages serially arranged;

a delay circuit having a predetermined time delay responsive to an output of said first plurality of stages;

a second plurality of stages serially arranged and responsive to said delay circuit; and

a selector in communication with said delay circuit to adjust the predetermined time delay.

26. An apparatus according to Claim 25,

wherein the first plurality of stages are arranged in a plurality of groups, wherein each of said plurality of groups comprises at least one of said first plurality of stages, and

wherein said apparatus comprises a plurality of LMS engines, each of said plurality of LMS engines corresponding to each of plurality of groups to provide weighting coefficients.

27. An apparatus according to Claim 26,

wherein one of said plurality of groups is arranged in plural subgroups, and

wherein one of the plurality of LMS engines corresponding to said one of said plurality of groups comprises at least one LMS engine each corresponding to each one of said plural subgroups to provide weighting coefficients.

28. An echo canceller comprising:

an input for receiving an input signal;

an FIR filter including:

a first plurality of stages serially arranged;

a delay circuit having a predetermined time delay responsive to an output of said first plurality of stages;

a second plurality of stages serially arranged and responsive to said delay circuit; and

a selector in communication with said delay circuit to adjust the predetermined time delay.

29. An echo canceller according to Claim 28,

wherein the first plurality of stages are arranged in a plurality of groups, wherein each of said plurality of groups comprises at least one of said first plurality of stages, and

wherein said apparatus comprises a plurality of LMS engines, each of said plurality of LMS engines corresponding to each of plurality of groups to provide weighting coefficients.

30. An echo canceller according to Claim 28,

wherein one of said plurality of groups is arranged in plural subgroups, and

wherein one of the plurality of LMS engines corresponding to said one of said plurality of groups comprises at least one LMS engine each corresponding to each one of said plural subgroups to provide weighting coefficients.

31. An Ethernet transceiver, comprising:

an Ethernet signal input;

an Ethernet signal output; and

an FIR filter including:

a first plurality of stages serially arranged;

a delay circuit having a predetermined time delay responsive to an output of said first plurality of stages;

a second plurality of stages serially arranged and responsive to said delay circuit; and

a selector in communication with said delay circuit to adjust the predetermined time delay.

32. An Ethernet transceiver according to Claim 31,

wherein the first plurality of stages are arranged in a plurality of groups, wherein each of said plurality of groups comprises at least one of said first plurality of stages, and

wherein said apparatus comprises a plurality of LMS engines, each of said plurality of LMS engines corresponding to each of plurality of groups to provide weighting coefficients.

33. An Ethernet transceiver according to Claim 31,

wherein one of said plurality of groups is arranged in plural subgroups, and

wherein one of the plurality of LMS engines corresponding to said one of said plurality of groups comprises at least one LMS engine each corresponding to each one of said plural subgroups to provide weighting coefficients.

34. FIR filter apparatus comprising:

input means for receiving an input signal;

FIR filter means for filtering the input signal received by said input means comprising three filter stages; and

first delay means for delaying a signal between two of said three filter stages by a first time delay;

second delay means for delaying a signal between another two of said three filter stages by a second time delay, wherein the first time delay and second time delay are different.

35. An apparatus according to Claim 34, wherein the second time delay of said second delay means is adjustable.

36. FIR filter apparatus comprising:

a first plurality of filter means for filtering a signal serially arranged;

delay means for delaying an output of said first plurality of filter means by a predetermined time delay;

a second plurality of filter means for filtering a signal from said delay means; and

selector means for adjusting the predetermined time delay.

37. An apparatus according to Claim 36,

wherein the first plurality of filter means are arranged in a plurality of groups, wherein each of said plurality of groups comprises at least one of said first plurality of stages, and

wherein said apparatus comprises a plurality of LMS means, each of said plurality of LMS means corresponding to each of plurality of groups for providing weighting coefficients.

38. An apparatus according to Claim 37,

wherein one of said plurality of groups is arranged in plural subgroups, and

wherein one of the plurality of LMS means corresponding to said one of said plurality of groups comprises at least one LMS means each corresponding to each one of said plural subgroups for providing weighting coefficients.

39. A method for filtering a signal comprising the steps of:

a) receiving an input signal;

b) multiplying the input signal received in step (a) by a first coefficient;

c) delaying the input signal received in step (a) by a first time delay;

d) multiplying a signal from step (c) by a second coefficient;

e) adding a signal from step (b) to a signal from step (d)

f) delaying a signal received in step (c) by a second time delay, wherein the first time delay is different than the second time delay;

g) multiplying a signal from step (f) by a third coefficient; and

h) adding a signal from step (e) to a signal from step (g).

40. A method for filtering a signal comprising the steps of:

a) receiving an input signal;

b) multiplying the input signal received in step (a) by a first coefficient;

c) delaying a signal from step (a) by a first time delay;

d) multiplying a signal from step (c) by a second coefficient;

e) delaying a signal from step (d) by a second time delay, wherein the first time delay is different than the second time delay;

f) adding a signal from step (b) to a signal from step (e)
g) multiplying the signal from step (c) by a third coefficient;
h) delaying a signal in step (g) by the second time delay; and
i) adding a signal from step (h) to the signal from step (d).

41. A method according to Claim 39 or 40, further comprising the step of adjusting the second time delay.

42. A method according to Claim 39 or 40, Further comprising the step of providing a test signal as the input signal.

43. A computer program for filtering a signal comprising the steps of:
a) receiving an input signal;
b) multiplying the input signal received in step (a) by a first coefficient;
c) delaying the input signal received in step (a) by a first time delay;
d) multiplying a signal from step (c) by a second coefficient;
e) adding a signal from step (b) to a signal from step (d)
f) delaying a signal received in step (c) by a second time delay, wherein the first time delay is different than the second time delay;
g) multiplying a signal from step (f) by a third coefficient; and

h) adding a signal from step (e) to a signal from step (g).

44. A computer program for filtering a signal comprising the steps of:

a) receiving an input signal;

b) multiplying the input signal received in step (a) by a first coefficient;

c) delaying a signal from step (a) by a first time delay;

d) multiplying a signal from step (c) by a second coefficient;

e) delaying a signal from step (d) by a second time delay, wherein the first time delay is different than the second time delay;

f) adding a signal from step (b) to a signal from step (e)

g) multiplying a signal from step (c) by a third coefficient;

h) delaying the input signal received in step (g) by the second time delay; and

i) adding a signal from step (h) to the signal from step (d).

45. A computer program according to Claim 43 or 44, further comprising the step of adjusting the second time delay.

46. A computer program according to Claim 43 or 44, further comprising the step of providing a test signal as the input signal.